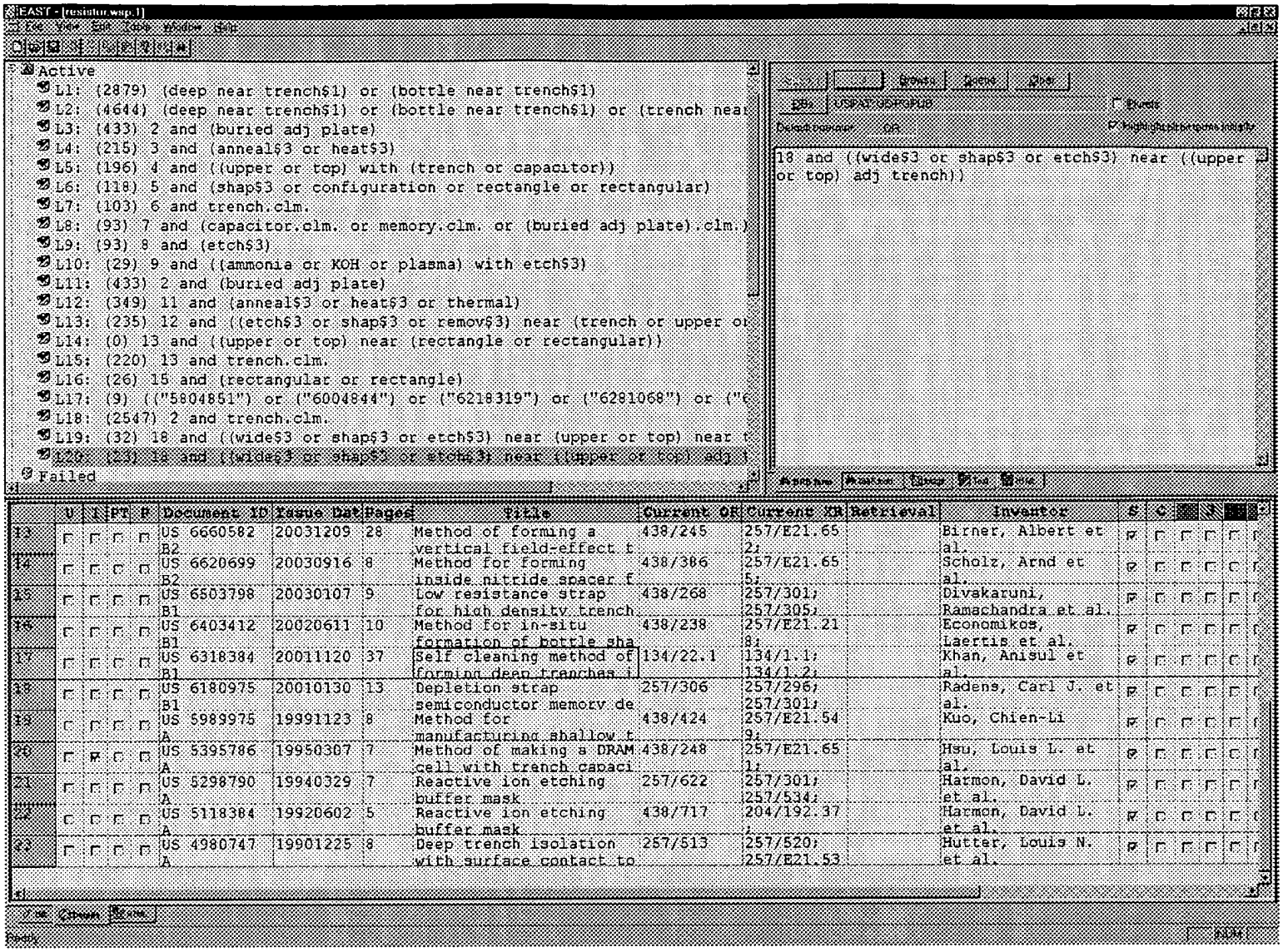

	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C	3
13					US 6660582 B2	20031209	28	Method of forming a vertical field-effect t	438/245	257/E21.652;		Birner, Albert et al.			
14					US 6620699 B2	20030916	8	Method for forming inside nitride spacer f	438/306	257/E21.655;		Scholz, Arnd et al.			
15					US 6503798 B1	20030107	9	Low resistance strap for high density trench	438/268	257/301; 257/305;		Divakaruni, Ramachandra et al.			
16					US 6403412 B1	20020611	10	Method for in-situ formation of bottle sha	438/238	257/E21.218;		Economikos, Laertis et al.			
17					US 6318384 B1	20011120	37	Self cleaning method of forming deep trenches i	134/22.1	134/1.1; 134/1.2;		Khan, Anisul et al.			
18					US 6180975 B1	20010130	13	Depletion strap semiconductor memory de	257/306	257/296; 257/301;		Radens, Carl J. et al.			
19					US 5989975 A	19991123	8	Method for manufacturing shallow t	438/424	257/E21.549;		Kuo, Chien-Li			
20					US 5395786 A	19950307	7	Method of making a DRAM cell with trench capaci	438/248	257/E21.651;		Hsu, Louis L. et al.			
21					US 5298790 A	19940329	7	Reactive ion etching buffer mask	257/622	257/301; 257/534;		Harmon, David L. et al.			
22					US 5118384 A	19920602	5	Reactive ion etching buffer mask	438/717	204/192.37;		Harmon, David L. et al.			
23					US 4980747 A	19901225	8	Deep trench isolation with surface contact to	257/513	257/520; 257/E21.538		Hutter, Louis N. et al.			

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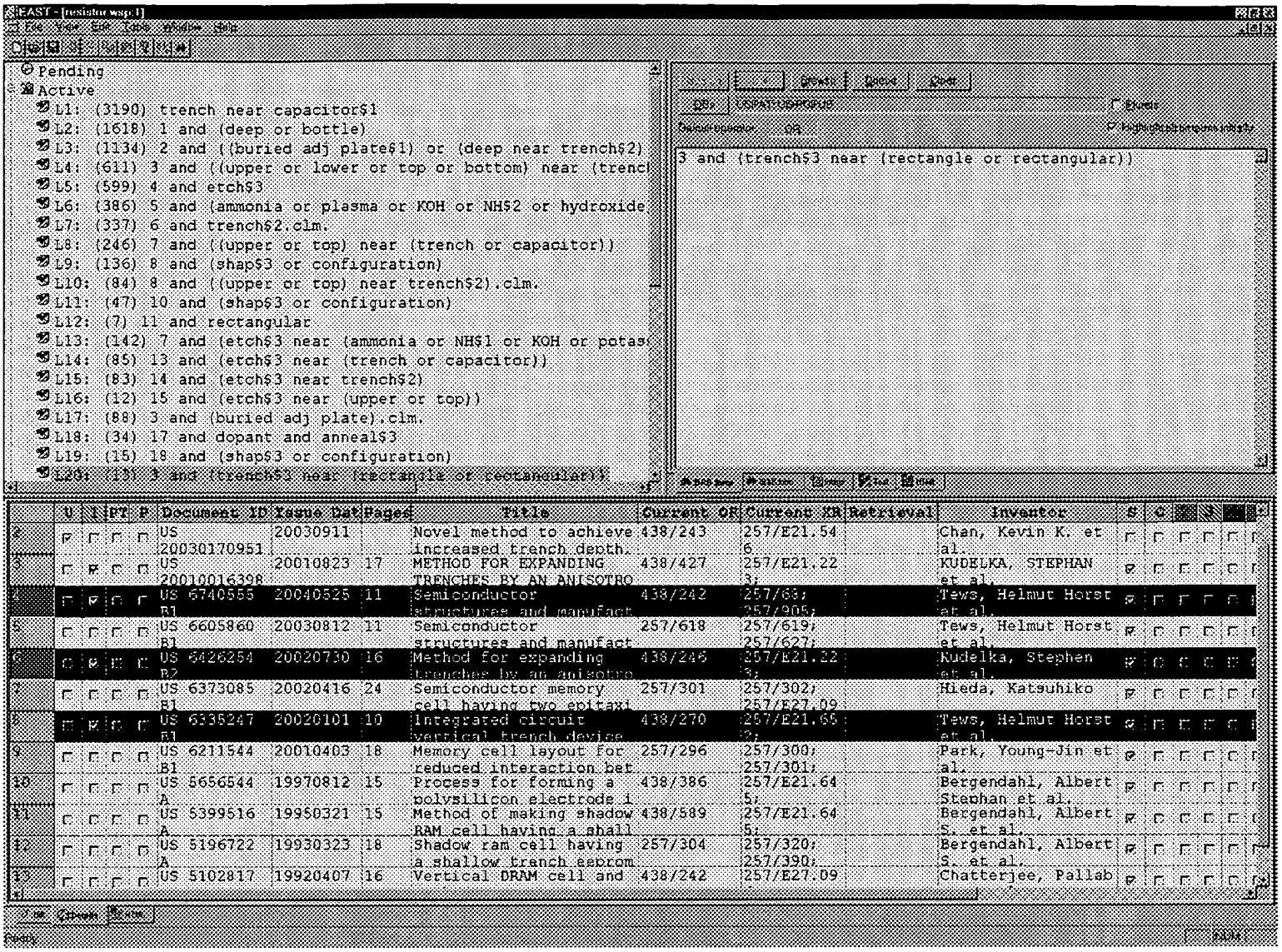

	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S
4	☑	☐	☐	☐	US 20030170951	20030911		Novel method to achieve increased trench depth.	438/243	257/E21.546		Chan, Kevin K. et al.	☐
3	☐	☑	☐	☐	US 20010016398	20010823	17	METHOD FOR EXPANDING TRENCHES BY AN ANISOTRO	438/427	257/E21.223;		KUDELKA, STEPHAN et al.	☑
2	☐	☑	☐	☐	US 6740555 B1	20040525	11	Semiconductor structures and manufact	438/242	257/68; 257/905;		Tews, Helmut Horst et al.	☑
5	☐	☐	☐	☐	US 6605860 B1	20030812	11	Semiconductor structures and manufact	257/618	257/619; 257/627;		Tews, Helmut Horst et al.	☑
6	☐	☑	☐	☐	US 6426254 B2	20020730	16	Method for expanding trenches by an anisotro	438/246	257/E21.223;		Kudelka, Stephen et al.	☑
7	☐	☐	☐	☐	US 6373085 B1	20020416	24	Semiconductor memory cell having two epitaxi	257/301	257/302; 257/E27.09		Hieda, Katsuhiko	☑
8	☐	☑	☐	☐	US 6335247 B1	20020101	10	Integrated circuit vertical trench device	438/270	257/E21.662;		Tews, Helmut Horst et al.	☑
9	☐	☐	☐	☐	US 6211544 B1	20010403	18	Memory cell layout for reduced interaction bet	257/296	257/300; 257/301;		Park, Young-Jin et al.	☑
10	☐	☐	☐	☐	US 5656544 A	19970812	15	Process for forming a polysilicon electrode i	438/386	257/E21.645;		Bergendahl, Albert Stephan et al.	☑
11	☐	☐	☐	☐	US 5399516 A	19950321	15	Method of making shadow RAM cell having a shall	438/589	257/E21.645;		Bergendahl, Albert S. et al.	☑
12	☐	☐	☐	☐	US 5196722 A	19930323	18	Shadow ram cell having a shallow trench eeprom	257/304	257/320; 257/390;		Bergendahl, Albert S. et al.	☑
13	☐	☐	☐	☐	US 5102817	19920407	16	Vertical DRAM cell and	438/242	257/E27.09		Chatterjee, Pallab	☑